Modeling and Analysis Techniques for System-Level Architectural Design of Telecom Front-Ends

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Invited Paper

***Abstract*—An overview is presented of the challenges and design issues in the system-level design of mixed analog–digital telecom front-ends. The progress in very large scale integration technology allows the integration of complex systems on a chip, containing both analog and digital parts. In order to boost the design productivity and guarantee the optimality of such systems while meeting the time-to-market constraints, a systematic top-down design approach has to be followed with sufficient time and attention paid to system-level architectural design before proceeding to the detailed block or circuit design. This paper will present high-level system exploration tools that allow to analyze architectural alternatives for the telecom front-end and to explore system tradeoffs such as finding the optimal analog–digital partitioning. This will be illustrated with results from experimental tools. Finally, the crucial underlying technology for such high-level design will be described in detail: analog behavioral modeling, efficient high-level simulation methods, and analog power/area estimation.**

***Index Terms*—RF modeling and simulation, telecom system exploration and architectual design.**

I. Introduction

ADVANCES in deep submicrometer very large scale integration (VLSI) integrated circuit processing technologies offer designers the possibility to integrate more and more functionality on one and the same die, enabling in the near future the integration of complete systems that before occupied one or more printed circuit boards onto a single piece of silicon [1], [2]. An increasing part of these integrated systems contain digital as well as analog circuits, and this is in application areas like telecommunications, automotive and multimedia among others [3].

The drive toward integrated mixed-signal analog/digital integrated circuits (ICs), however, is posing certain big problems. The complexity of the systems that can be integrated on a single IC can only be mastered by using advanced computer-aided design (CAD) tools and by shifting to a higher level of design abstraction [4]. A typical top-down design flow for mixed-signal integrated systems may look as shown in Fig. 1, where the following distinct phases can be identified: system specification, architectural design, cell design, cell layout, and system layout [5]–[9].

For the digital circuits, commercial simulation and synthesis tools, especially at the logic and layout level, have been around for some years now, and a considerable part of the digital design flow has been automated, starting the design from a register transfer level (RTL) description. In recent years, the design entry level has been shifting more and more toward an object-oriented system description. Most of the current system design environments, however, cannot handle the analog circuits, thereby excluding the possibility to explore system-level tradeoffs and architectural decisions across the analog–digital boundary. For instance, in telecom applications like GSM, WLAN, and xDSL, the analog front-end circuits are limiting the overall performance of the system and proper system architectural decisions can substantially relax the requirements on the analog interface circuits.

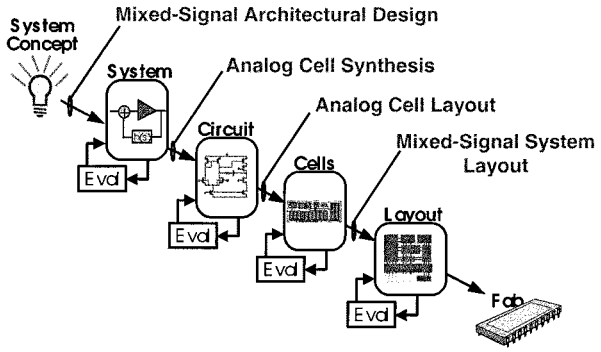

Fig. 1. Top-down view of the mixed-signal IC design process.

The growing interest in mixed-signal ICs is also exposing the lack of mature analog CAD tools that can boost the productivity of analog designers. Therefore, although the analog circuits typically occupy only a small part of the area in mixed-signal ICs, they require a disproportionally large part of the overall design time. In times of increased integration with uniform deadlines for the analog and digital parts, this poses serious challenges to the analog designers and their productivity, prompting them to adopt some form of CAD support or even synthesis [5]. It has been reported that the use of analog CAD tools can drastically reduce the design time, without sacrificing performance [10].

In summary, some of the major challenges in mixed-signal integrated system design today are as follows:

- the need for a mixed-signal architectural exploration environment allowing the analysis and comparison of different architectural solutions in terms of performance, power, and area;

Manuscript received April 30, 2001.

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Publisher Item Identifier S 0018-9480(02)00845-1.

- the fact that such an environment inevitably also requires higher level analog modeling and power/area estimation to quantify and compare the different system solutions;
- the need for analog CAD and synthesis tools to boost the analog design productivity up to a level compatible with the present time-to-market constraints;
- the need for a full set of mixed-signal signal integrity analysis and design tools that can cope with the complexity of fully integrated systems.

This overview paper will describe a systematic design methodology for the top-down design and bottom-up verification of telecom front-ends from architecture to circuit. Section II will describe the architectural-level design methodology which translates system-level specifications into an architecture and a set of specifications for all the building blocks. This will be illustrated with examples of architectural-level exploration and design of telecom front-ends, including also the problem of analog–digital partitioning. Section III will then describe the crucial underlying technology for such high-level design: analog behavioral modeling, efficient high-level simulation methods, and analog power/area estimation. Finally, conclusions will be drawn in Section IV.

II. Mixed-Signal Architectural System Exploration

The general objective of analog architectural system exploration is twofold. First of all, a proper architecture for the system has to be decided upon. Secondly, the required specifications for each of the blocks in the chosen architecture must be determined, so that the overall system meets its requirements at a minimum implementation cost. The aim of a system exploration environment is to provide the system designer with the platform and the supporting tool set to explore in a short time different architectural alternatives and to take the above decisions based on quantified rather than heuristic information. Compared to commercial solutions such as SIMULINK or ADS, that are increasingly used in industry today for system-level simulations, more efficient and especially more accurate methods are needed that also provide quantitative data on power or chip area budgets.

Consider for instance the digital telecommunication link of Fig. 2. It is clear that digital bits are going into the link to be transmitted over the channel, and that the received signals are being converted again in digital bits. One of the main considerations in digital telecom design is the bit error rate, which characterizes the reliability of the link. This bit error rate is impacted by the characteristics of the transmission channel itself, but also by the architecture chosen for the transmitter and receiver front-end and by the performances achieved by the subblocks. For example, the noise figure and nonlinear distortion of the input low-noise amplifier are key parameters. Similarly, the resolution and sampling speed of the used analog-to-digital converter (ADC) may have a large influence on the bit error rate (BER), but this also determines the requirements for the other analog subblocks. A higher ADC resolution may relax the filtering requirements in the transceiver, resulting in simpler filter structures, but it will also consume more power and chip area than a lower resolution converter. However, the minimum required

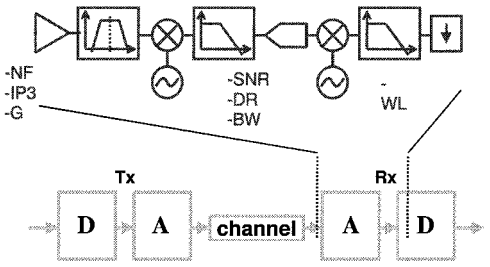

Fig. 2. Digital telecommunication link, indicating a possible receiver front-end architecture with some block specifications.

ADC resolution and therefore also the minimum power and area depend on the architecture chosen for the transceiver front-end. Clearly, there is a large interaction between system-level architectural decisions and the performance requirements for the different subblocks, which on their turn are bounded by technological limits that shift with every new technology process being employed.

In general, analog high-level design consists of the translation of system-level specifications into a proper architecture of subblocks, in which the individual specifications of all subblocks are completely decided so that the overall system meets its specifications [6]. However, during the top-down design phase the subblocks are not yet device-level circuit implementations. Hence, they have to be represented as "behavioral models" representing their functional input–output behavior. The performance can be evaluated by carrying out a behavioral simulation of the architecture and/or by evaluating—if available—a set of equations that describes the architecture's performances in terms of the subblock specifications [11]. If equations can be obtained, this approach is in general faster, but the simulation-based approach with high-level model representations for the subblocks is more generally applicable. In this way, the performance of an architecture with given building block specifications can be analyzed by the system designer and checked against the system specifications.

This approach of analog system-level architectural exploration will first be illustrated with some examples. The important underlying techniques—simulation algorithms, behavioral models, and power/area estimators—will then be described afterwards.

A. Transceiver Front-End Exploration and Optimization

Our first experimental prototype tool toward the architectural-level exploration and optimization of receiver front-ends was the ORCA tool [12]. The tool focused on receivers as their design is more difficult due to the uncertainty and wide range of possible input signals (such as desired channel, noise, neighboring channels, and blocking signals). The tool contains a library of behavioral models and power estimation functions for the typical blocks encountered in receivers. The behavioral model of each block includes both its nominal behavior (amplification, filtering, mixing) as well as its most important nonidealities (e.g., noise, distortion, aliasing, phase noise).

In ORCA the simulations were performed with a dedicated frequency-domain simulation algorithm that processes stochastic input power spectra typical for the targeted application

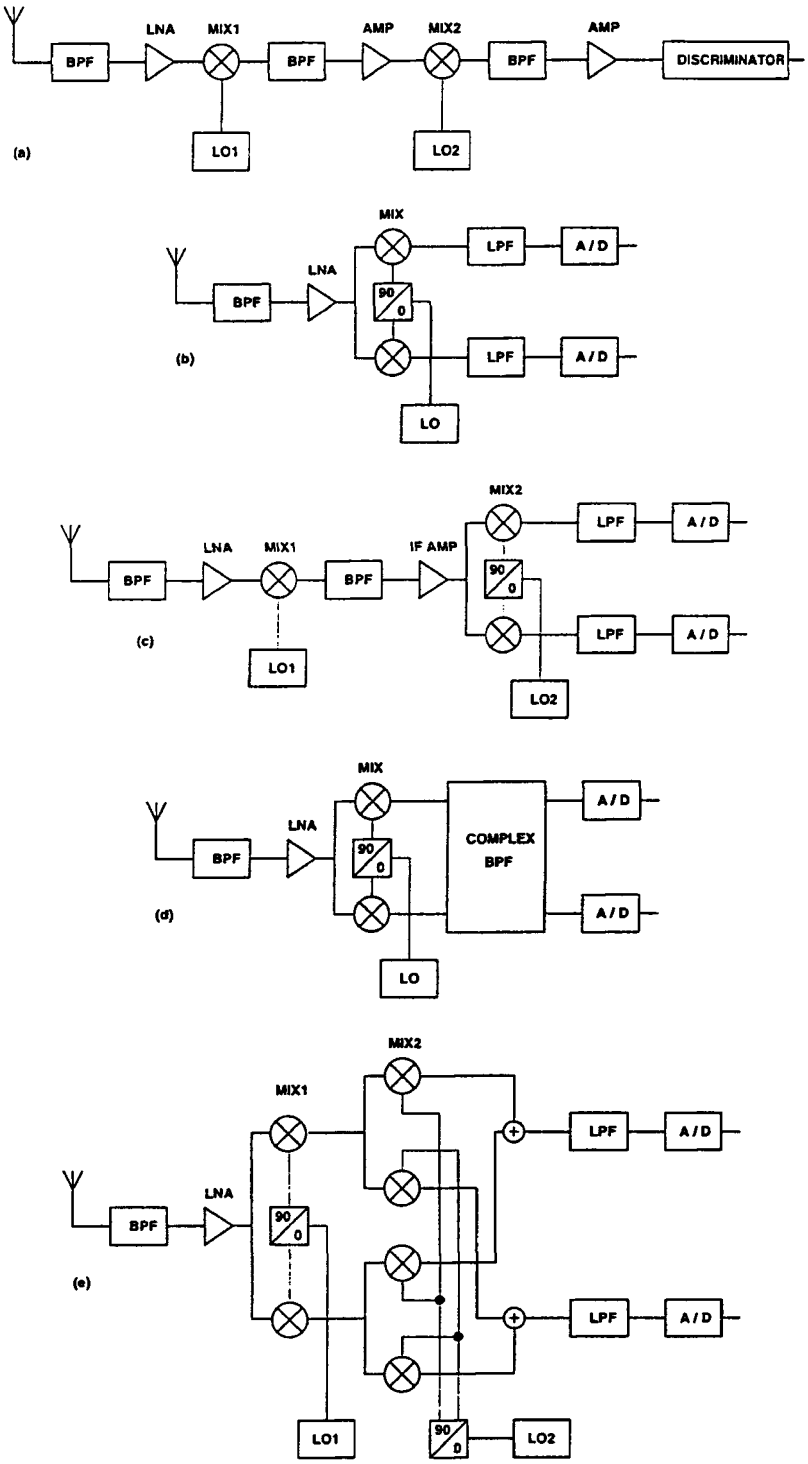

Fig. 3. Different RF receiver architectures. (a) Classical double-IF receiver. (b) Zero-IF receiver. (c) Combined IF zero-IF receiver. (d) Low-IF receiver. (e) Quasi-IF receiver architecture.

(e.g., GSM, DECT) [11], [12]. The power spectral distributions at every node in the circuit were calculated in an efficient though approximate way to enable a short ORCA response time to the designer during the architectural exploration phase of the receiver. The tool allowed the designer to interactively explore alternative receiver architectures and to investigate design tradeoffs within each architecture at the architectural level, before designing each individual subblock. As the performance analysis routine was also integrated within an optimization loop, the tool could also perform an optimal high-level synthesis of a given architecture toward a specific application such that the complete receiver meets the requiredsignal quality while the overall estimated power consumption of the entire architecture is minimized [12].

The recent boom of wireless communication applications has resulted in a demand for very small, highly integrated RF

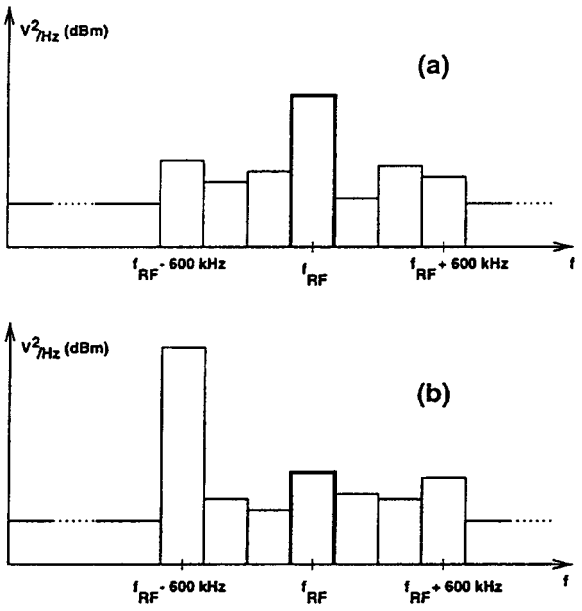

Fig. 4. Typical input power spectra for cellular phone applications.

transceivers dissipating low power. To achieve this goal, several new transceiver architectures different from the classical superheterodyne receiver have been proposed in recent years. Fig. 3(a)–(e) shows some of these architectures, i.e.: (a) the classical double-IF architecture, (b) the direct conversion or zero-IF architecture, (c) the combined IF zero-IF architecture, (d) the low-IF architecture with complex signal processing, and (e) the quasi-IF architecture. These architectures can then be analyzed by ORCA for input power spectra typical for their application, for instance the spectra shown in Fig. 4 for cellular phone applications (e.g., GSM).

As a first example, for the architecture of Fig. 3(c) and for the input spectrum of Fig. 4(a), the resulting spectrum at the receiver output as calculated by ORCA is shown in Fig. 5 [11]. The signal band of interest in this example is 100 kHz. The different channels have been approximated as rectangular spectra. The power spectrum of the wanted signal and the different signal-degrading effects (thermal and phase noise contributions from the subblocks, aliased signals and distortion introduced by the subblocks) are calculated and displayed separately by ORCA, allowing to analyze the different effects separately. The resulting signal-to-noise-and-distortion ratio (SNDR) in the signal band due to the different effects are summarized in Table I. The reliability of these results of course depends on the accuracy of the behavioral models, the employed signal representations and the simulation algorithms.

As a second example, consider a front-end for a cable TV (CATV) modem receiver, based on the MCNS standard [11]. The MCNS frequency band for upstream communication on the CATV network is from 5 to 42 MHz (extended subsplit band). Two architectures are shown in Fig. 6: an all-digital architecture where both the channel selection and the downconversion are done in the digital domain, and the classical architecture where the channel selection is performed in the analog domain. A typical input spectrum is shown in Fig. 7. For this example, we have used 12 QAM-16 channels with a 3-MHz

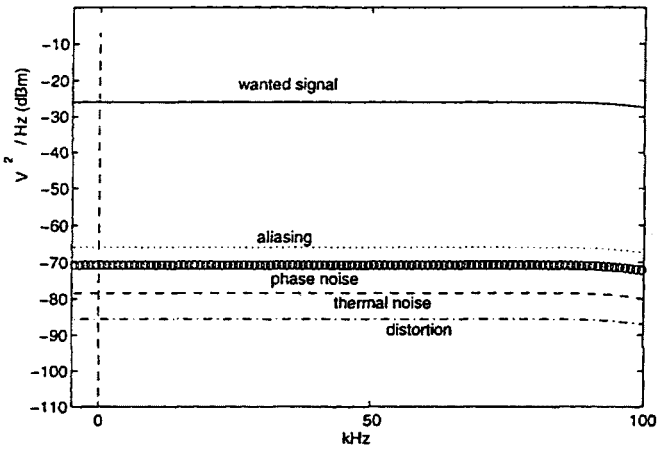

Fig. 5. Plot of an ORCA behavioral simulation result showing separately the receiver output spectrum with desired signal and major signal-degrading effects.

TABLE I
CONTRIBUTION OF THE DIFFERENT SIGNAL-DEGRADING EFFECTS TO THE OVERALL SNDR

	SNDR (dB)
thermal noise only	52.5
phase noise only	44.8
aliasing only	39.9
distortion only	59.9
DC peak	25.8
total (without DC peak)	38.8

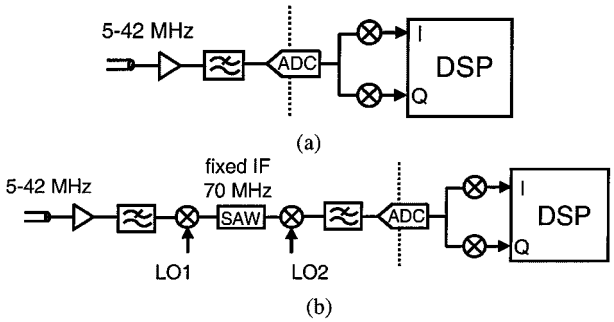

Fig. 6. Two architectures for CATV application. (a) All-digital architecture. (b) Classical architecture.

bandwidth. We assume a signal variation of the different channels of maximally ± 5 dB around the average level. The average channel noise is 30 dB below this level. Figs. 8 and 9 show the spectrum simulated by ORCA for the all-digital architecture of Fig. 6(a). Fig. 8 shows the spectrum after the ADC, whereas Fig. 9 shows the spectrum at the output after digital channel selection and quadrature downconversion. The wanted signal and the effects of the channel noise, the ADC quantization noise, and the second- and third-order distortion are shown separately. The resulting SNDR is equal to 22.7 dB in this case, which corresponds to a symbol error rate of less than 10^{-10} for QAM-16.

B. Architectural Exploration and Tradeoff Analysis

By performing the same analysis for different architectures and by linking the required subblock specifications to the power

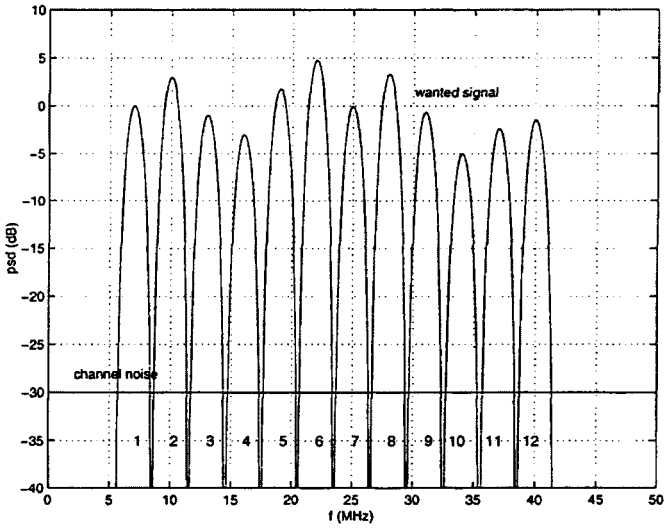

Fig. 7. Typical input spectrum for a CATV front-end architecture using 12 QAM-16 channels.

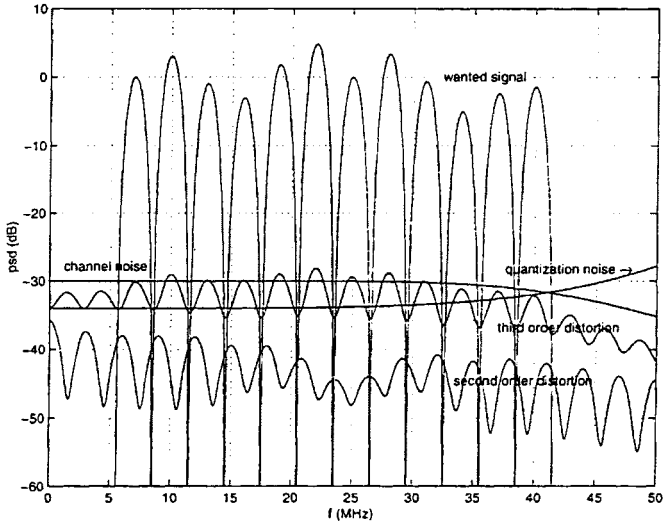

Fig. 8. Simulated spectrum of the all-digital CATV architecture after the ADC.

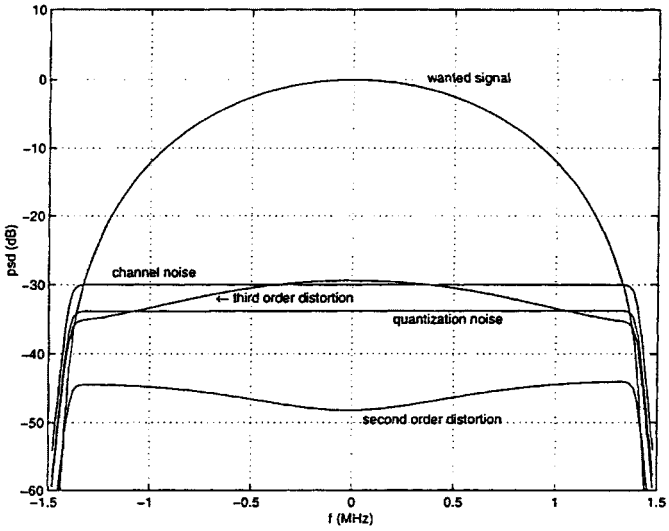

Fig. 9. Simulated spectrum of the all-digital CATV architecture at the receiver output.

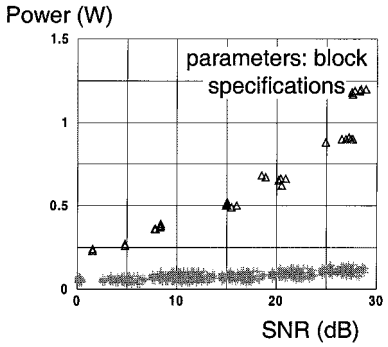

Fig. 10. Power consumption comparison between the all-digital CATV architecture (triangles) and the classical architecture (crosses) as a function of the required SNR.

and/or chip area required to implement the subblocks, a quantitative comparison of different alternative architectures becomes possible with respect to: 1) their suitability to implement the system specifications and 2) the corresponding implementation cost in power consumption and/or silicon real estate. To assess the latter, high-level power and/or area estimators must be used to quantify the implementation cost. In this way, the system designer can choose the most promising architecture.

Fig. 10 shows a comparison between the estimated total power consumption required by the all-digital and by the classical CATV receiver architectures of Fig. 6 as a function of the required SNR [13]. These results were obtained with the simulator FAST [14], which is a data-flow simulator for telecom front-ends. Clearly, with the current state of the technology, the classical architecture still requires much less power than the all-digital solution.

C. Analog–Digital System-Level Partitioning

Another important problem in mixed-signal system design is finding the optimal partitioning between analog and digital signal processing subblocks [15]. Today this partitioning is often performed *ad hoc*, with some crude calculations, by an experienced system designer. It is, however, often not feasible to investigate many alternative solutions in the design space. Also, although there might be good reasons for implementing as many functions in the digital domain as possible, two problems might result. Firstly, the specification constraints on the few remaining analog subblocks might become too stringent to realize them in the given technology. For instance, the required ADC specifications in terms of resolution and bandwidth might become unrealizable. Secondly, the digital solution might require more power than the solution with more analog functionality. That is exactly the reason why high-level exploration is useful to quantitatively find the optimal analog–digital partitioning in mixed-signal systems. Optimal here means for instance lowest overall power consumption for the complete system. Tools like ORCA can find the optimal partitioning by also incorporating architectural variations within the optimization variables. The method is intended to assist system designers with quantitative data in their comparing different alternative system architectures.

This is now illustrated for the baseband signal processing part of a direct conversion receiver as shown in Fig. 11. The parti-

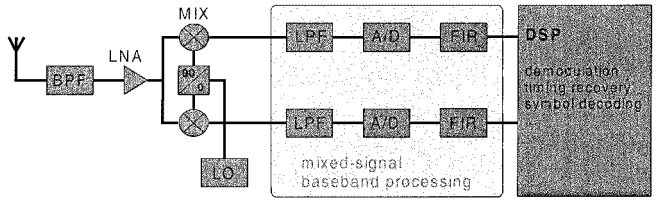

Fig. 11. Baseband signal processing channel in a direct conversion receiver.

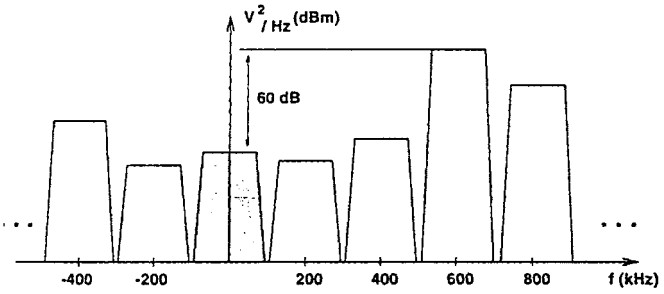

Fig. 12. Input spectrum of the baseband (channel) filtering blocks.

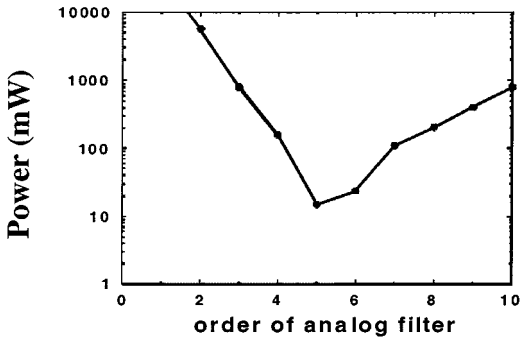

Fig. 13. Power consumption of the baseband signal processing channel as a function of the amount of analog filtering (and inversely the amount of digital filtering).

tioning tradeoff is in the position of the ADC and the amount of filtering in the analog versus the digital domain. Hence, the order of the analog low-pass filter and of the digital finite impulse response (FIR) filter are the architectural optimization variables. Subblock specifications include for instance the resolution and the speed of the ADC. The main system-level specification to be met is a 10-dB signal-to-noise requirement at the output of the digital multirate filter for an input signal spectrum to the baseband filtering blocks shown in Fig. 12. The system is simulated using the ORCA tool [12], extended with behavioral simulation models for digital (multirate) filters.

The resulting (estimated) power consumption varies as a function of the order of the analog filter (and inversely also of the digital filter), as shown in Fig. 13. The smallest overall power consumption is obtained with a fifth-order analog filter and correspondingly a 28-tap digital filter. Hence, this also determines the optimal insertion point of the ADC in the given technology. Clearly a lot of power can be gained by carefully making the tradeoff between analog and digital filtering in this example. The reliability of these results of course depends on the accuracy of the employed behavioral models, signal representations, simulation algorithms, and power estimators. Note also that the optimum will shift if other technology processes are used, since, for instance, the power estimations are a function of the technology parameters.

III. Underlying Technology: Behavioral Modeling, Simulation Algorithms, and Power Estimation

This section will now discuss in more detail the underlying technology needed for this mixed-signal system-level exploration: analog behavioral models, simulation algorithms and signal representations, and power estimators.

A. Analog Behavioral Modeling for System Exploration

A crucial element for system-level top-down design to succeed is the availability of analog behavioral models that describe the behavior of an analog block without knowing the details of the underlying circuit implementation. These models must describe the desired behavior of the block, while still including the major nonidealities of real implementations with sufficient accuracy. For this purpose, a library of generic behavioral models can be developed for analog blocks that are frequently encountered in the targeted application domain.

For telecom front-ends, for instance, the following behavior can be included in every block's model (see Fig. 14) [11]:

- intended behavior, e.g., amplification for an LNA, filtering for a filter, frequency translation for a mixer, etc.;
- noise behavior introduced by the block—this could be specified by characteristics like the noise figure;
- phase noise introduced by some blocks like the local oscillator driving a mixer;
- distortion behavior introduced by the block—this could be specified by characteristics like the harmonic distortion or intercept point;
- undesired aliasing or mirroring of signals by some blocks like a mixer or an ADC.

A generalization for the compact modeling of the frequency-dependent nonlinear distortion of telecom front-end circuits using Volterra kernels has been presented recently [16]. The key problem, however, remains the development of a good mathematical description for the block behavior, for which no good systematic methods exist yet. For efficiency reasons, preference is given to explicit models without iteration.

B. System-Level Architectural Simulation Methods

The second crucial element for system-level exploration and optimization is an efficient way to evaluate the performance of the circuit. Analytic equations that explicitly characterize an architecture's behavior as a function of the subblock parameters are a fast alternative if they are available, but the most general solution is to use some sort of numerical simulation to evaluate the front-end performance. However, different simulation techniques can be used, and they vary widely in CPU time consumption for systems that contain both high-frequency signals (e.g., antenna signals in an RF application) and downconverted baseband signals.

A standard integration-based simulation like in SPICE [17] would be too time-consuming due to the tight time-step control dictated by the high-frequency signals and would also waste

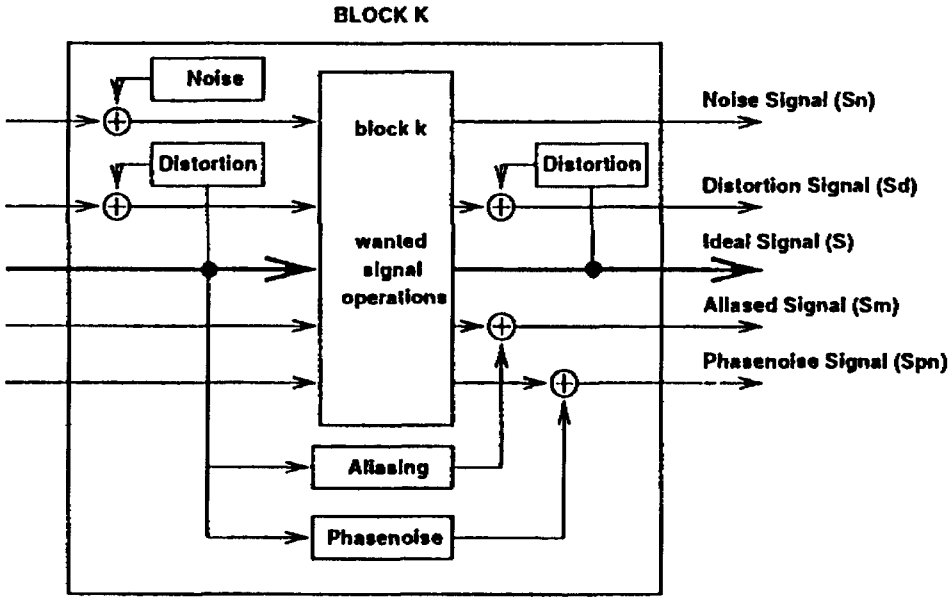

Fig. 14. General behavioral model template for an analog telecom front-end block.

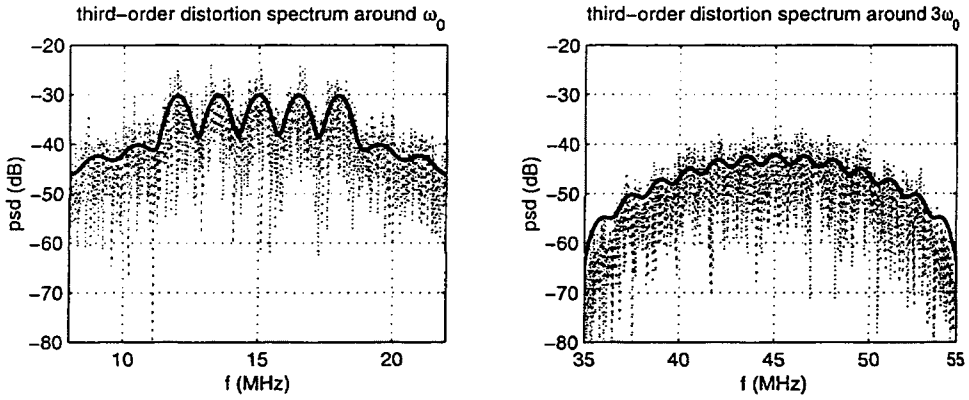

Fig. 15. Simulated results versus analytic expression approach (thick black line) of the third-order distortion spectrum for five QPSK-modulated channels.

much time simulating start-up transients before the steady-state situation is reached. Special RF simulation techniques like harmonic balance or shooting methods, on the other hand [18]–[22], directly calculate the steady-state solution in an efficient way, but they are interesting only for a small number of sinusoidal input tones, which is a poor approximation for complex digital telecom signals. Circuit envelope methods [23] can handle digital telecom signals more efficiently as they separate the calculation of the carrier and the modulating signal, but current commercial implementations are suboptimal as they treat all nodes in the system in the same global way. Similarly, multirate methods employing two time scales have recently been developed to analyze systems with widely different time constants [24].

To make system-level exploration really fast and interactive, dedicated algorithms have to be developed that speed up the calculations by maximally exploiting the properties of the signals and systems under investigation and by using proper approximations where possible. The ORCA tool, for example, represents the signals as a sum of bandlimited piecewise rational approximations [12]. This formulation requires less memory than a sampled data-point representation, and many of the signal operations can be performed symbolically. For example, if we assume that the input signals X to a block are a random process with zero-mean Gaussian distribution, which is a good approximation for multi-channel applications, then the power spectral densities of the second- and third-order distortion at the output Y can efficiently be calculated using

$$S_{Y_2}(f) = a_2^2(R_X^2(0)\delta(f) + 2(S_X(f) \otimes S_X(f))) \quad (1)$$

$$S_{Y_3}(f) = a_3^2(9R_X^2(0)S_X(f) + 6(S_X(f) \otimes S_X(f) \otimes S_X(f))) \quad (2)$$

where a_2 and a_3 are the second- and third-order nonlinearity coefficients, and R and S represent the autocorrelation and power spectral density functions, respectively. Fig. 15 shows a comparison between the results obtained using this analytic approach and the results from the time-domain simulation of a large number of independent QPSK symbols modulated on five different carriers. The figure shows a good agreement between the power spectral content of both cases for the third-order distortion output around two different frequencies.

A frequency-domain Volterra series-based behavioral simulation tool for RF systems was presented in [25]. It is restricted to weakly nonlinear systems, for which the Volterra series approximation holds. A more recent development is the FAST tool which performs a time-domain dataflow type of simulation without iterations [14] and which easily allows dataflow co-simulation with digital blocks. Compared to commercial simulators like COSSAP, PTOLEMY, or SPW, this simulator is more efficient by using block processing instead of point-by-point calculations for the different time points in circuits without feedback. In addition, the signals are represented as complex equivalent baseband signals with multiple carriers. The signal representation is local and fully optimized as the signal at each node in the circuit can have a set of multiple carriers and each corresponding equivalent baseband component can be sampled with a different time step depending on its bandwidth. Large feedback loops, especially when they contain nonlinearities, are however more difficult to handle with this approach. Fig. 10 was obtained with this FAST tool. A method to efficiently simulate BERs with this simulator has been presented in [26].

Finally, the FONZIE simulation environment is also fully adaptive in that it uses the most efficient signal representation at every node in the circuit depending on the block type [27]. Representations supported range from using damped complex exponentials as simulation basis functions, which is suited for the time-domain simulation of weakly nonlinear circuits, to using a sampled-data representation for strongly nonlinear circuits. The tool automatically converts from one representation to the other during the simulation.

C. Power Estimation Models

The last crucial element to compare different architectural alternatives and to explore tradeoffs in system-level exploration and optimization are accurate and efficient power and area estimators [28]–[30]. They allow to assess and compare the optimality of different design alternatives. Such estimators are functions that predict the power or area that is going to be consumed by a circuit implementation of an analog block (e.g., an ADC) with given specification values (e.g., resolution and speed). Since the implementation of the block is not yet know during high-level system design and considering the large number of different possible implementations for a block, it is very difficult to generate these estimators with high absolute accuracy. This however is not so important since the most crucial aspect to reliably compare different alternatives is their tracking accuracy with varying block specifications. Such estimators for example have been presented for high-speed ADCs in [28] and for continuous-time active filters in [29].

IV. Conclusion

This review paper has given an overview of the challenges and design issues in the system-level design of mixed analog–digital telecom front-ends. In order to achieve the design productivity and design optimality needed to design future systems on a chip within the tightening time-to-market constraints, a systematic top-down design approach has to be followed with sufficient time and attention paid to system-level architectural design before proceeding to the detailed block and circuit design. High-level system exploration tools have been presented that enable analog–digital co-design and that allow to analyze architectural alternatives and explore tradeoffs such as finding the optimal analog–digital partitioning. Examples of system-level architectural exploration for telecom front–ends, including analog–digital partitioning, have been given. Finally, the crucial underlying technologies needed for such high-level exploration have been described in detail: analog behavioral modeling, efficient high-level simulation methods and analog power/area estimation.

It can be concluded that a systematic top-down approach is unavoidable for designing future complex systems. Experimental tools to support such an approach at the architectural level have been described in this paper, but major challenges remain in the development of accurate yet efficient analog behavioral models and power/area estimators. Also, the mapping from system-level specifications (an “algorithm”) into an appropriate architecture remains an open problem; today it is still the designer who comes up with the different candidate system architectures.

Acknowledgment

The author acknowledges all Ph.D. students who have contributed to this paper’s research results, and in particular S. Donnay, Katholieke Universiteit Leuven, Leuven, Belgium, P. Vanassche, Katholieke Universiteit Leuven, Leuven, Belgium, and E. Lauwers, Katholieke Universiteit Leuven, Leuven, Belgium.

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